FIG.1

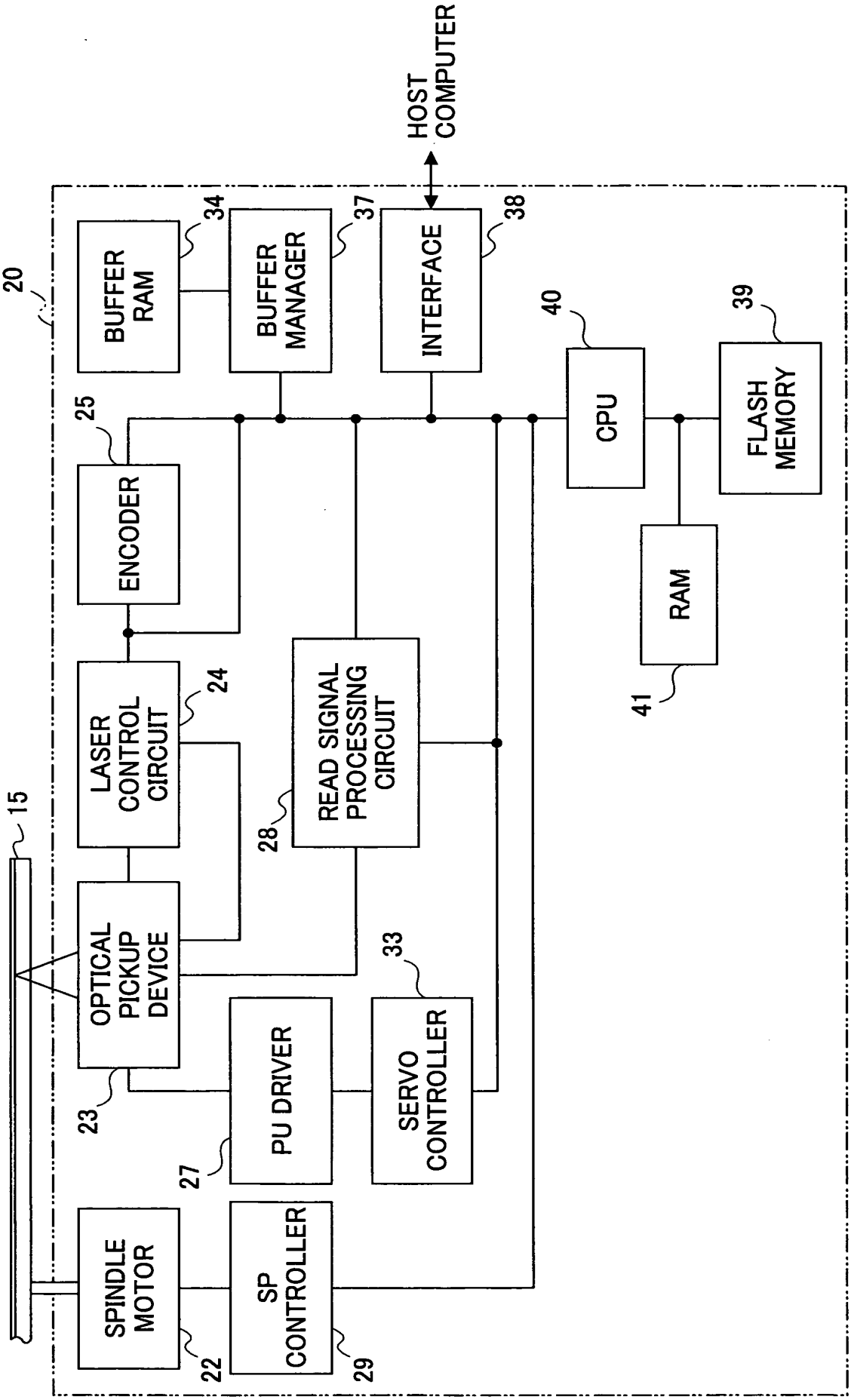

HOST COMPUTER
20
BUFFER RAM
34
BUFFER MANAGER
37
INTERFACE
38
40
CPU
39
FLASH MEMORY
25
ENCODER
RAM
41
LASER CONTROL CIRCUIT
24
READ SIGNAL PROCESSING CIRCUIT
28
15
OPTICAL PICKUP DEVICE
33
SERVO CONTROLLER
23
PU DRIVER
27
SPINDLE MOTOR
22
SP CONTROLLER
29

FIG.2

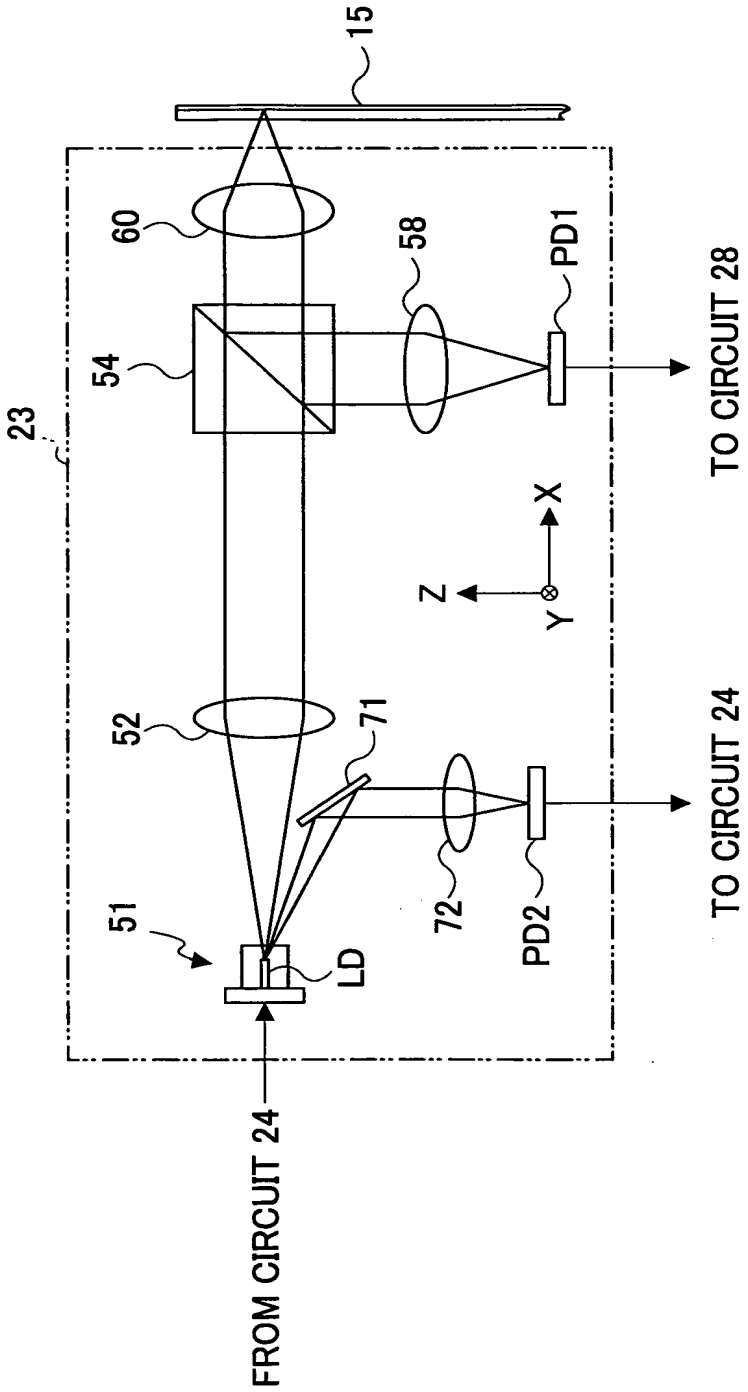

15
60
58
PD1
54
23
TO CIRCUIT 28
X
Z
Y
52
71
TO CIRCUIT 24
51
LD
72
PD2
FROM CIRCUIT 24

FIG.3

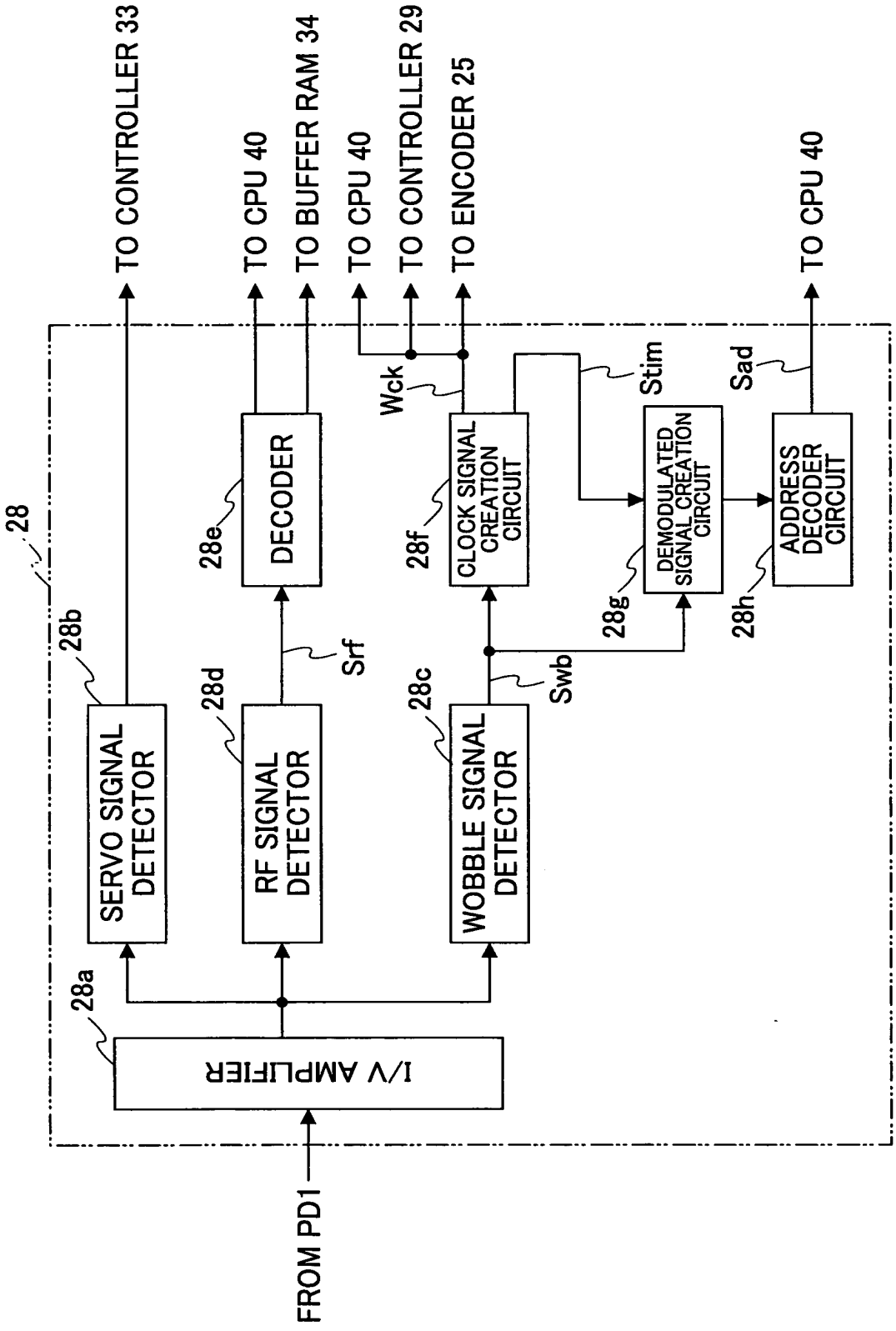

28
FROM PD1
I/V AMPLIFIER
28a
SERVO SIGNAL DETECTOR
28b
RF SIGNAL DETECTOR
28d
WOBBLE SIGNAL DETECTOR
28c
Srf
Swb
DECODER
28e
CLOCK SIGNAL CREATION CIRCUIT
28f
DEMODULATED SIGNAL CREATION CIRCUIT
28g
ADDRESS DECODER CIRCUIT
28h
Wck
Stim
Sad
TO CONTROLLER 33
TO CPU 40
TO BUFFER RAM 34
TO CPU 40
TO CONTROLLER 29
TO ENCODER 25
TO CPU 40

FIG.4

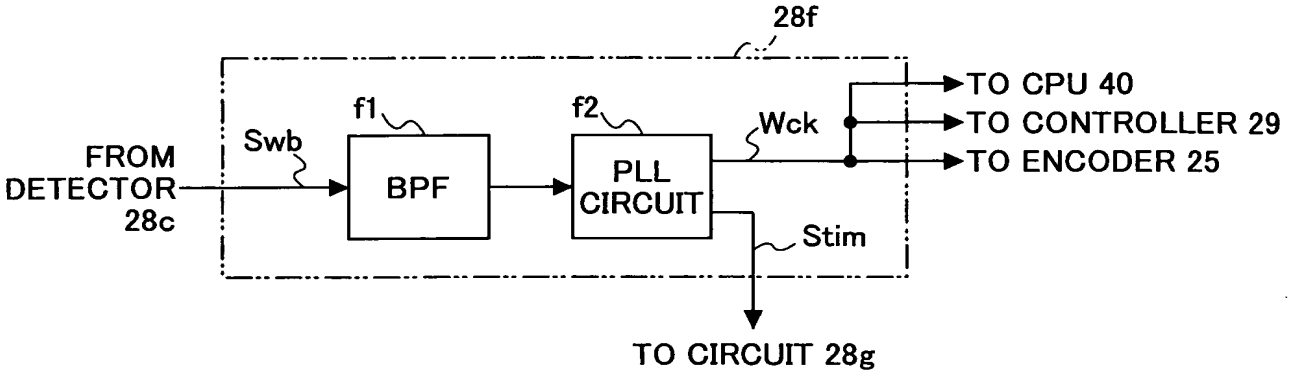

28f
f1
f2
Swb
Wck
FROM
DETECTOR
28c
BPF
PLL
CIRCUIT
TO CPU 40
TO CONTROLLER 29
TO ENCODER 25
Stim
TO CIRCUIT 28g

FIG.5

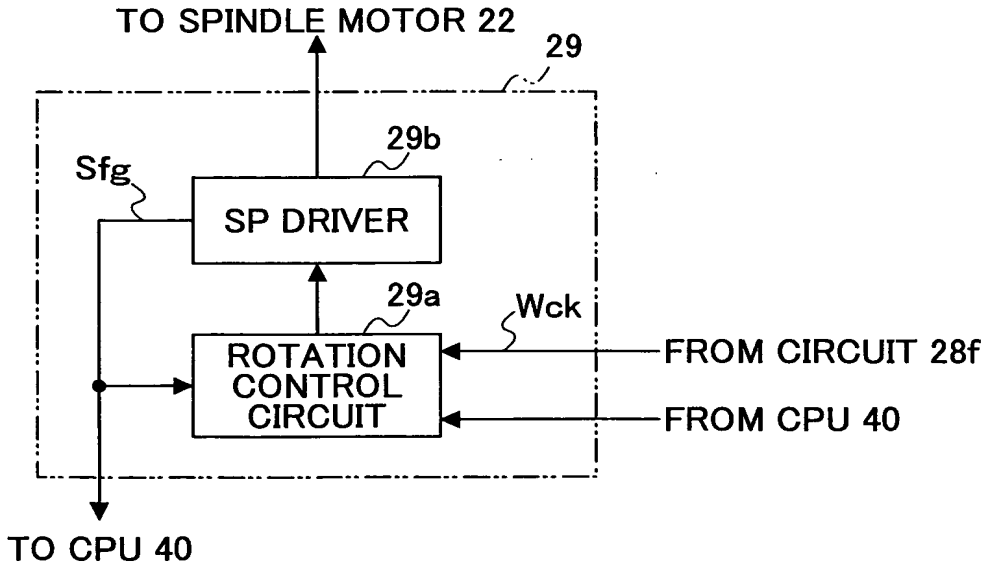

TO SPINDLE MOTOR 22
29
29b
Sfg
SP DRIVER
29a
Wck
ROTATION
CONTROL
CIRCUIT
FROM CIRCUIT 28f
FROM CPU 40
TO CPU 40

FIG.6

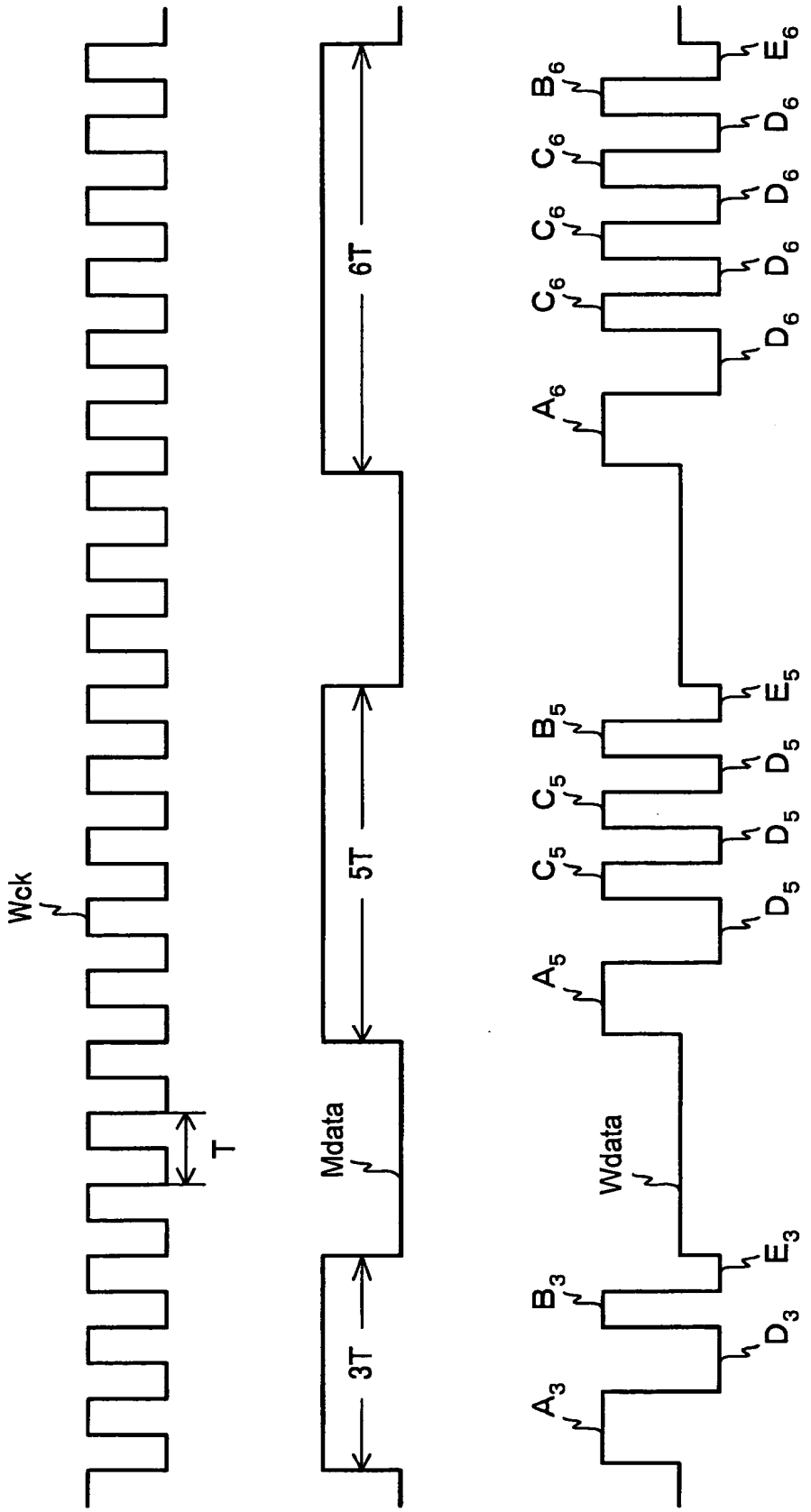

Wck
T
Mdata
3T
5T
6T
Wdata
A3
B3
D3
E3
A5
C5
D5
B5
D5
E5
A6
C6
D6
C6
D6
C6
D6
B6
D6
E6

FIG.7

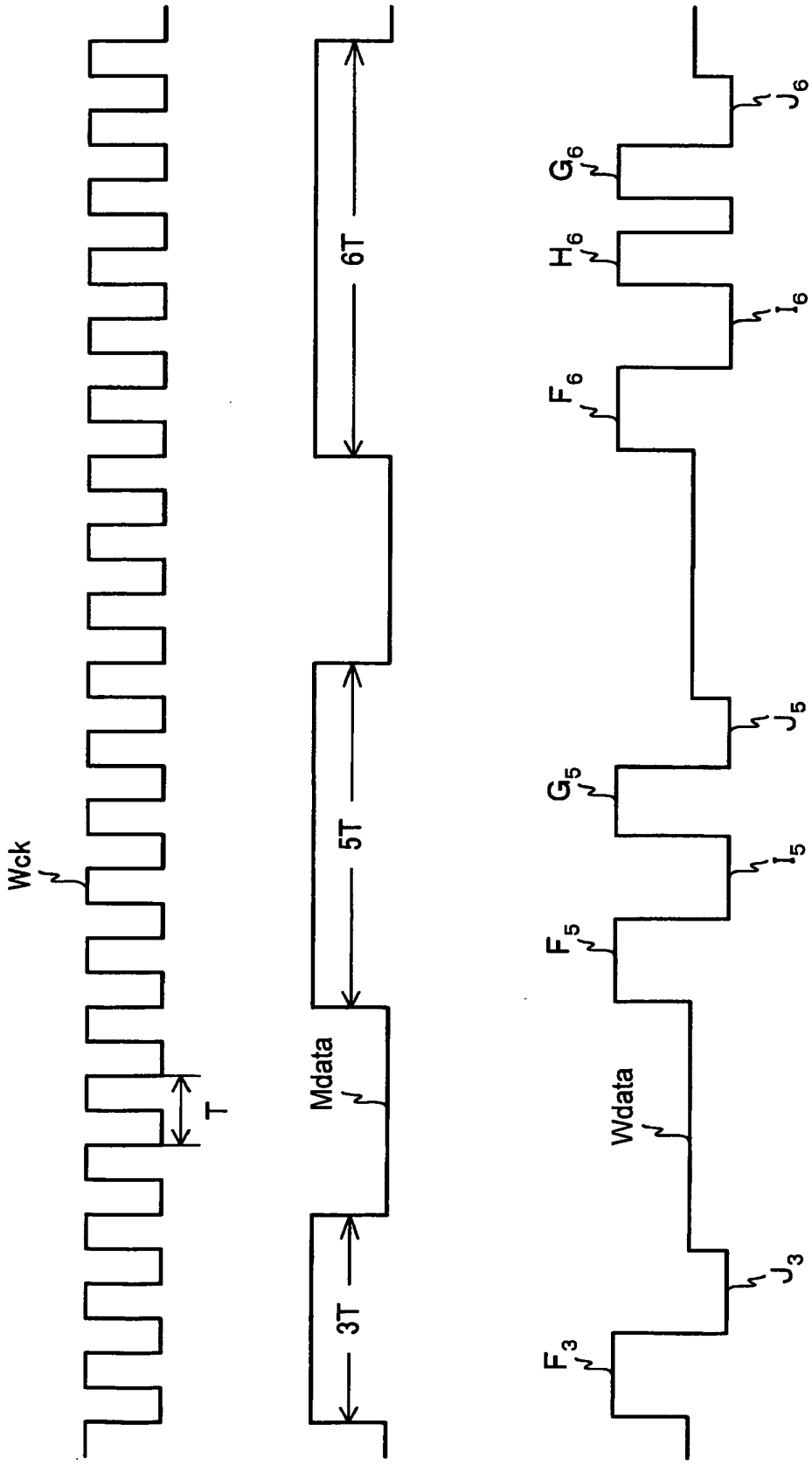


FIG.8

MARK LENGTH	PULSE NAME	TIMING	TYPE		
			TYPE 1	TYPE 2	.....
			1X SPEED	2X SPEED	.....
3T	A3	RISE	+1/32	+2/32	
		FALL	+1/32	+2/32	
	B3	RISE	+0/32	+1/32	
		FALL	+0/32	+1/32	
	D3	FALL	+0/32	+1/32	
		RISE	+0/32	+1/32	
	E3	FALL	+3/32	+3/32	
		RISE	+3/32	+4/32	
5T	A5	RISE	+1/32	+2/32	
		FALL	+1/32	+2/32	
	B5	RISE	+0/32	+1/32	
		FALL	+0/32	+1/32	
	C5	RISE	+0/32	+1/32	
		FALL	+0/32	+1/32	
	D5	FALL	+0/32	+1/32	
		RISE	+0/32	+1/32	
	E5	FALL	+2/32	+2/32	
		RISE	+2/32	+3/32	
.....	.....	.....	.....	.....	.....

FIG.9

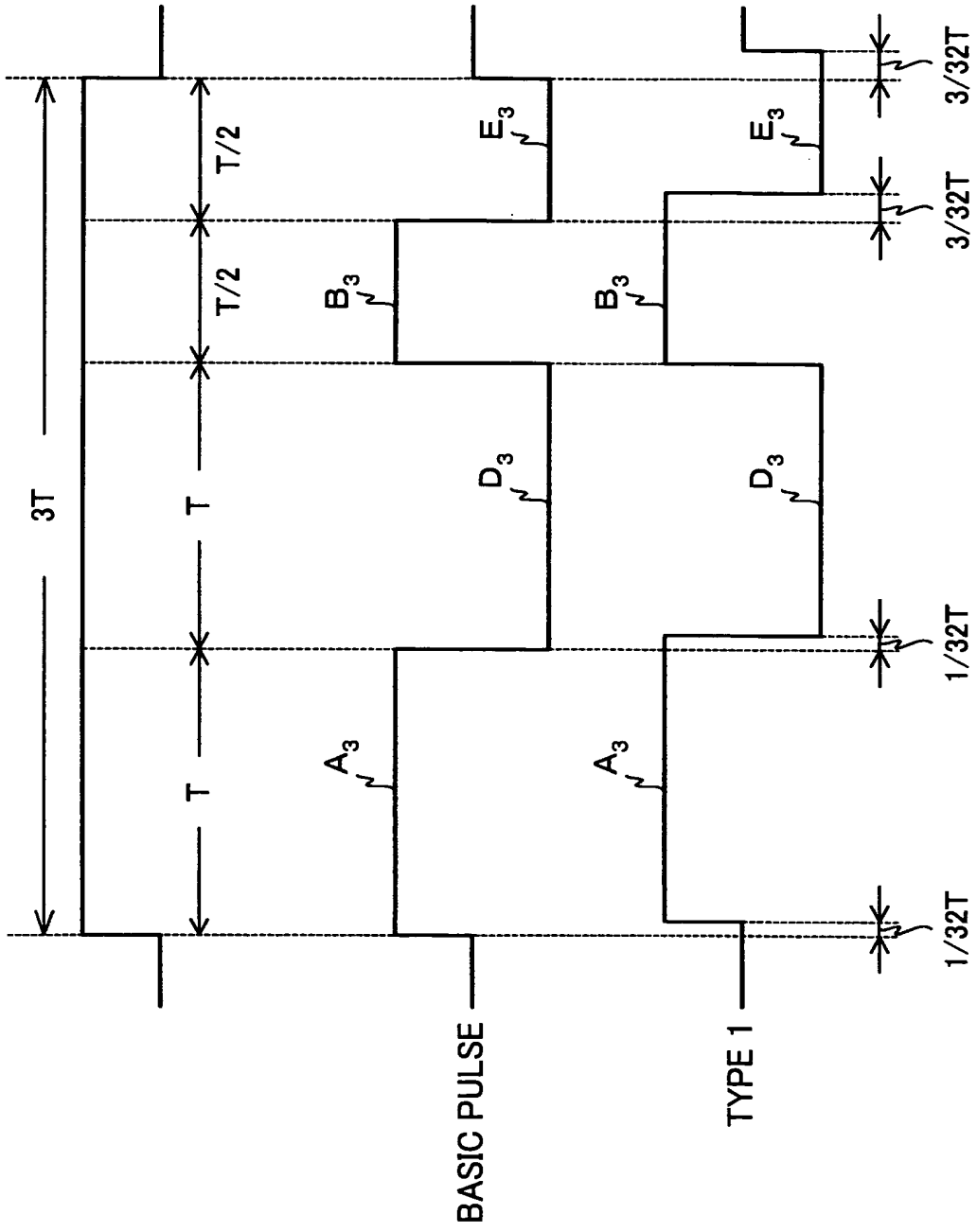

3T
T/2
T/2
T
T
A_3
B_3
D_3
E_3
A_3
B_3
D_3
E_3
1/32T
3/32T
3/32T
1/32T
BASIC PULSE
TYPE 1

FIG.10

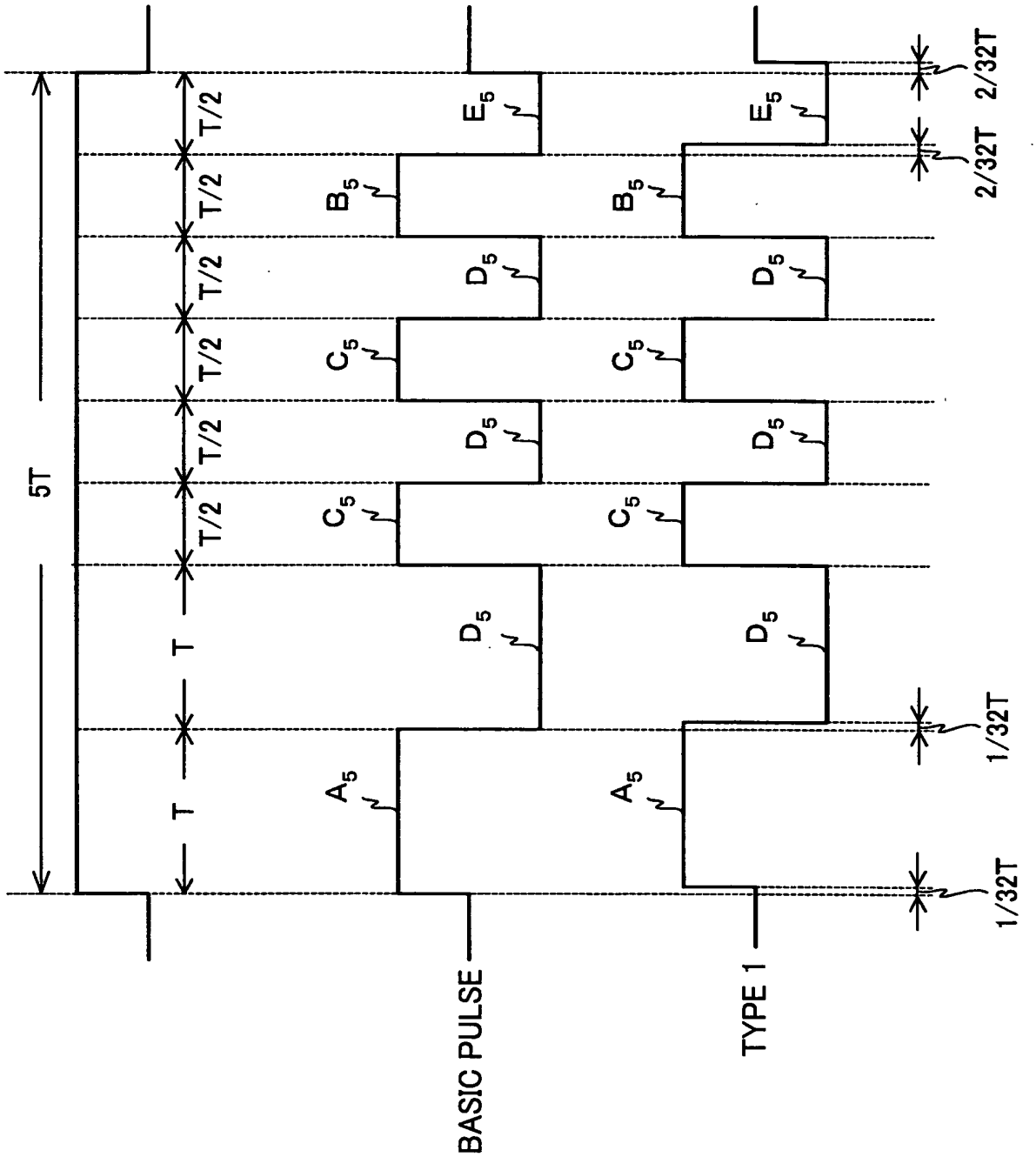


FIG.11

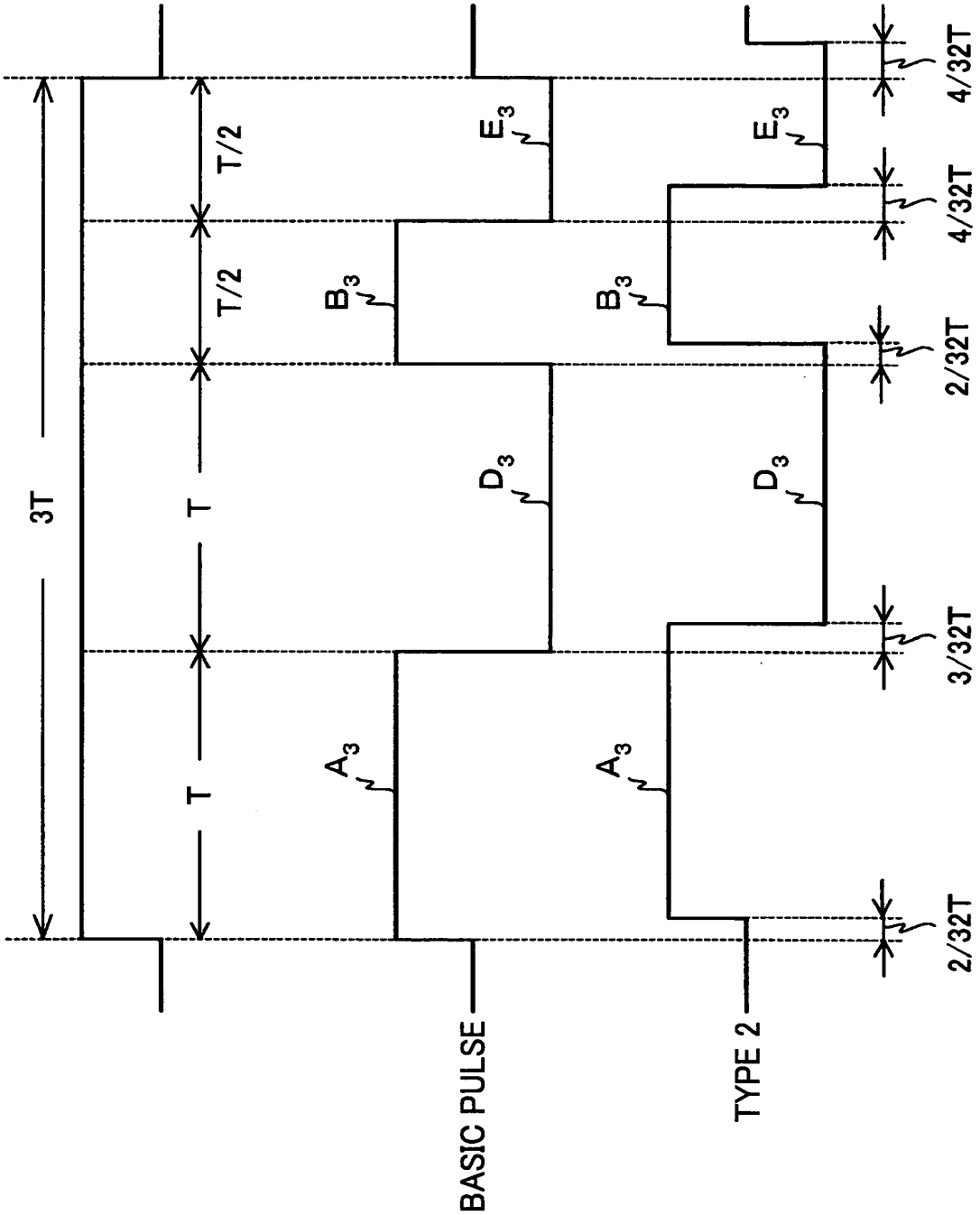

3T
T
T
T/2
T/2
A_3
B_3
D_3
E_3
A_3
B_3
D_3
E_3
BASIC PULSE
TYPE 2
2/32T
3/32T
2/32T
4/32T
4/32T

FIG.12

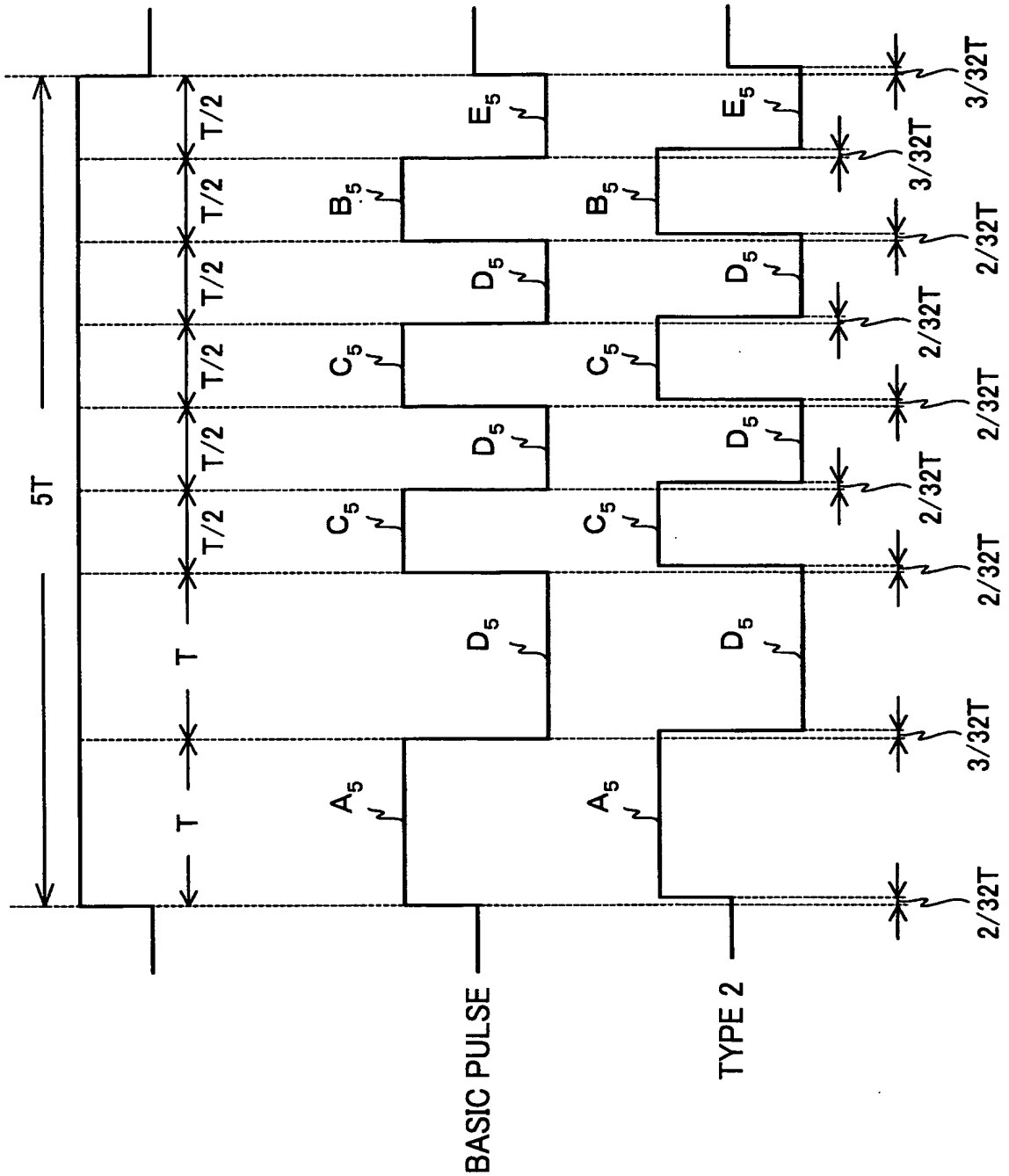


FIG.13

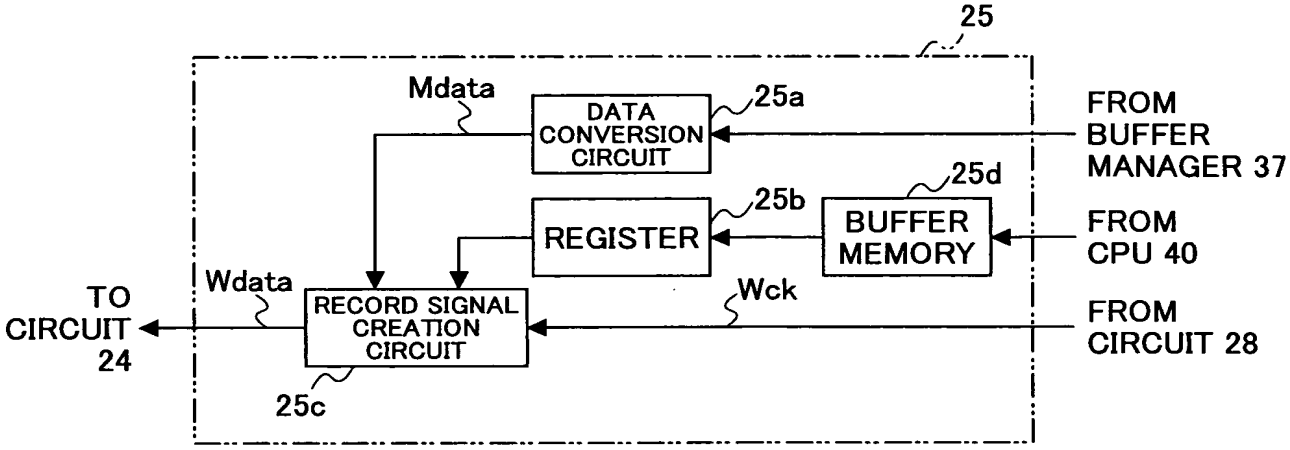

25
Mdata
DATA CONVERSION CIRCUIT
25a
FROM BUFFER MANAGER 37
25d
25b
REGISTER
BUFFER MEMORY
FROM CPU 40
Wdata
Wck
TO CIRCUIT 24
RECORD SIGNAL CREATION CIRCUIT
FROM CIRCUIT 28
25c

FIG.14

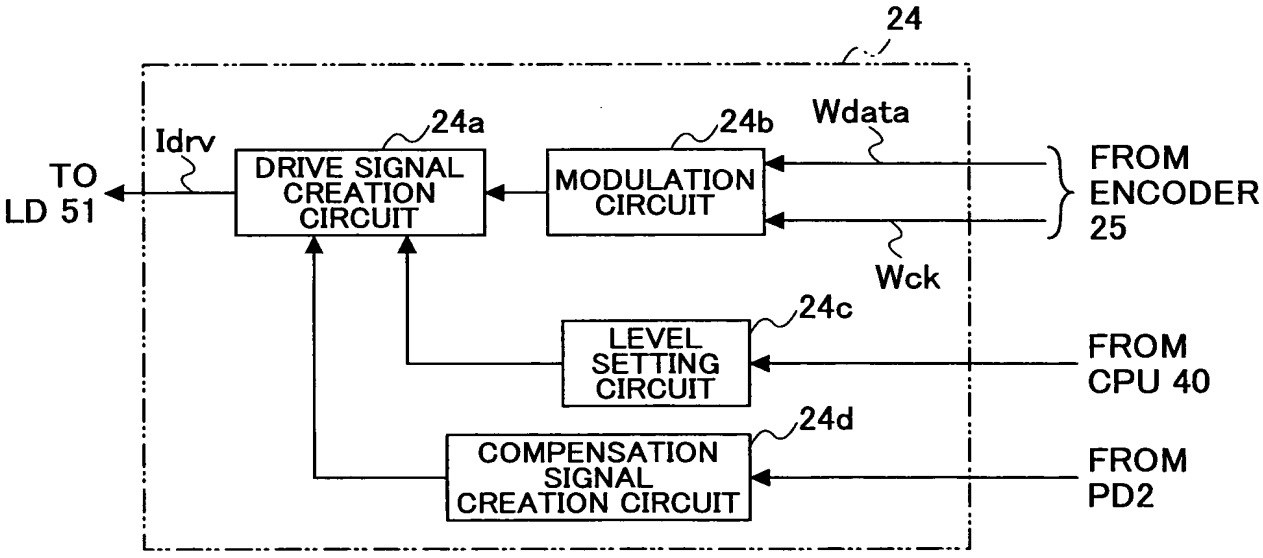

24
Idrv
24a
24b
Wdata
TO LD 51
DRIVE SIGNAL CREATION CIRCUIT
MODULATION CIRCUIT
FROM ENCODER 25
Wck
24c
LEVEL SETTING CIRCUIT
FROM CPU 40
24d
COMPENSATION SIGNAL CREATION CIRCUIT
FROM PD2

FIG.15

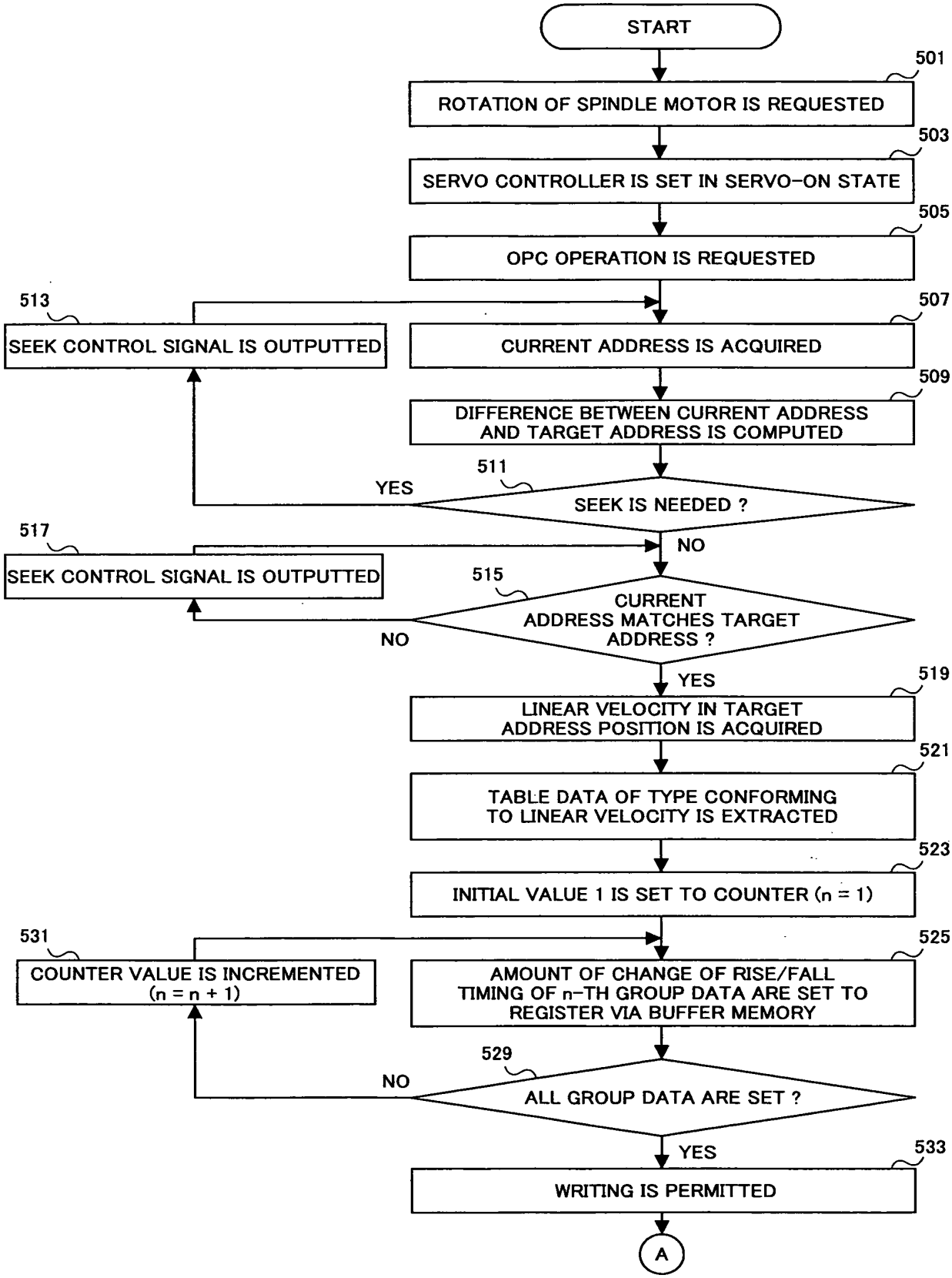

START
501
ROTATION OF SPINDLE MOTOR IS REQUESTED
503
SERVO CONTROLLER IS SET IN SERVO-ON STATE
505
OPC OPERATION IS REQUESTED
513
SEEK CONTROL SIGNAL IS OUTPUTTED
507
CURRENT ADDRESS IS ACQUIRED
509
DIFFERENCE BETWEEN CURRENT ADDRESS AND TARGET ADDRESS IS COMPUTED
511
YES
SEEK IS NEEDED ?
NO
517
SEEK CONTROL SIGNAL IS OUTPUTTED
515
CURRENT ADDRESS MATCHES TARGET ADDRESS ?
NO
YES
519
LINEAR VELOCITY IN TARGET ADDRESS POSITION IS ACQUIRED
521
TABLE DATA OF TYPE CONFORMING TO LINEAR VELOCITY IS EXTRACTED
523
INITIAL VALUE 1 IS SET TO COUNTER (n = 1)
531
COUNTER VALUE IS INCREMENTED (n = n + 1)
525
AMOUNT OF CHANGE OF RISE/FALL TIMING OF n-TH GROUP DATA ARE SET TO REGISTER VIA BUFFER MEMORY
529
NO
ALL GROUP DATA ARE SET ?
YES
533
WRITING IS PERMITTED
A

FIG.16

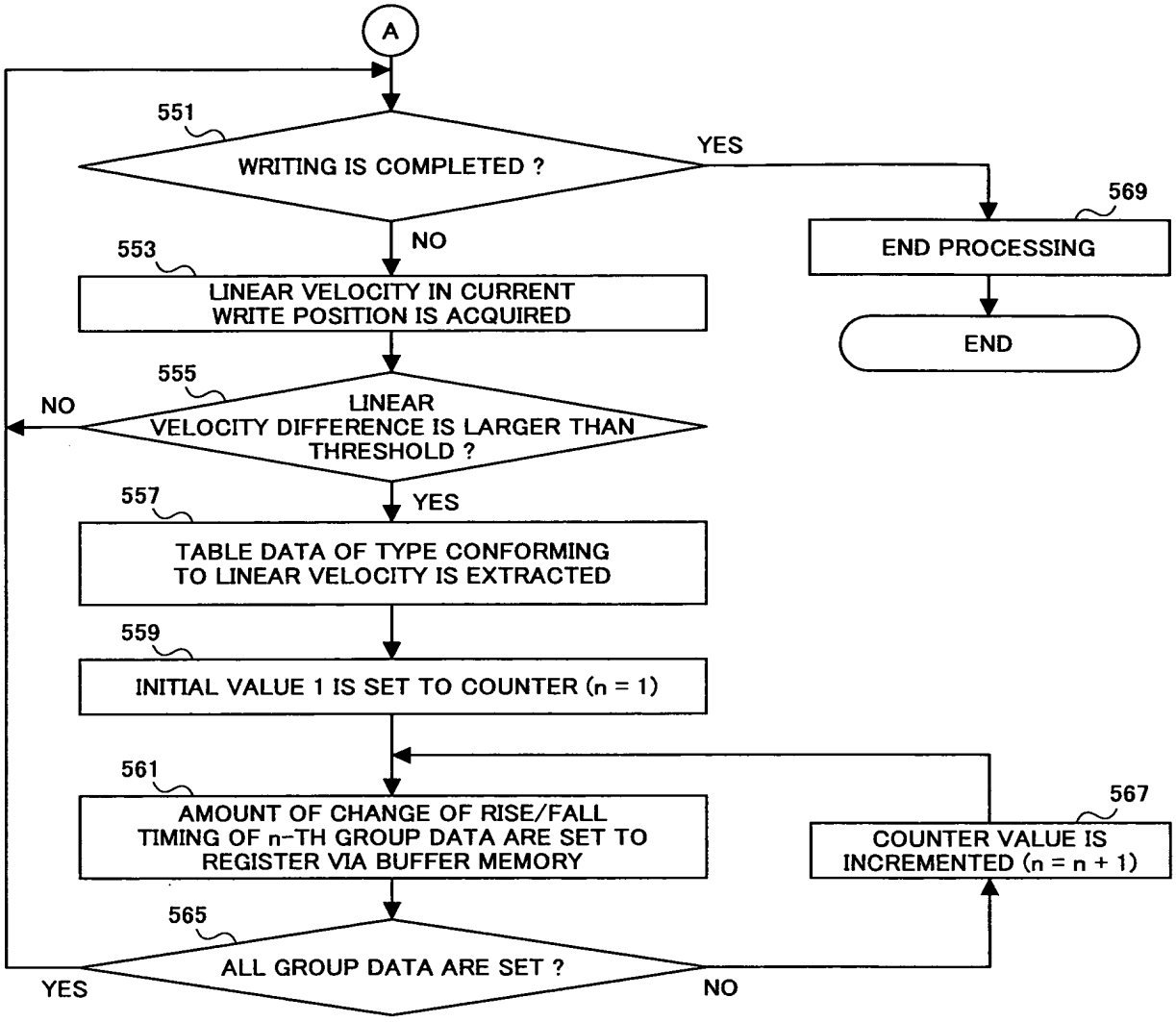

A
551
WRITING IS COMPLETED ?
YES
NO
569
END PROCESSING
END
553
LINEAR VELOCITY IN CURRENT WRITE POSITION IS ACQUIRED
555
LINEAR VELOCITY DIFFERENCE IS LARGER THAN THRESHOLD ?
NO
YES
557
TABLE DATA OF TYPE CONFORMING TO LINEAR VELOCITY IS EXTRACTED
559
INITIAL VALUE 1 IS SET TO COUNTER (n = 1)
561
AMOUNT OF CHANGE OF RISE/FALL TIMING OF n-TH GROUP DATA ARE SET TO REGISTER VIA BUFFER MEMORY
567
COUNTER VALUE IS INCREMENTED (n = n + 1)
565
ALL GROUP DATA ARE SET ?
YES
NO

FIG.17

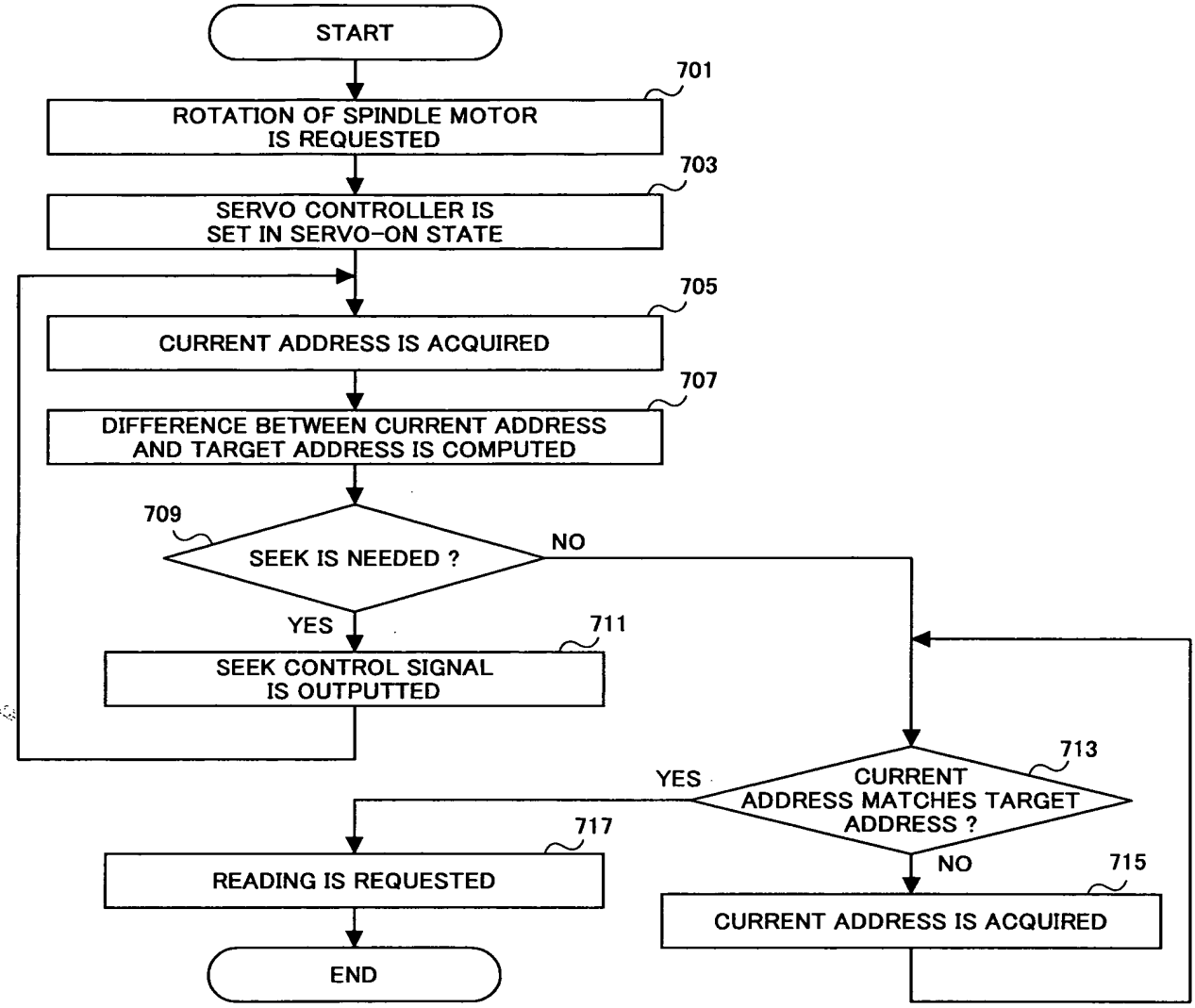
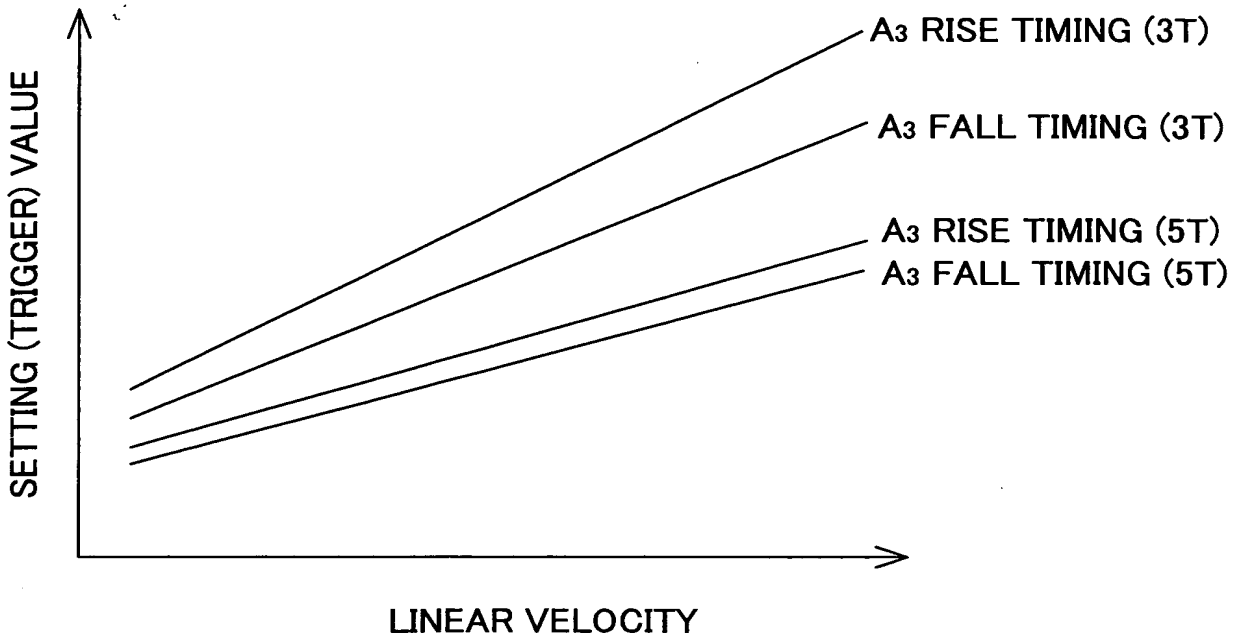

START
701
ROTATION OF SPINDLE MOTOR IS REQUESTED
703
SERVO CONTROLLER IS SET IN SERVO-ON STATE
705
CURRENT ADDRESS IS ACQUIRED
707
DIFFERENCE BETWEEN CURRENT ADDRESS AND TARGET ADDRESS IS COMPUTED
709
SEEK IS NEEDED ?
NO
YES
711
SEEK CONTROL SIGNAL IS OUTPUTTED
713
CURRENT ADDRESS MATCHES TARGET ADDRESS ?
YES
NO
715
CURRENT ADDRESS IS ACQUIRED
717
READING IS REQUESTED
END

FIG.18


A3 RISE TIMING (3T)
A3 FALL TIMING (3T)
A3 RISE TIMING (5T)
A3 FALL TIMING (5T)
SETTING (TRIGGER) VALUE
LINEAR VELOCITY